Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: CrNiAg**

**G = .020” X .022”**

**S = .070” X .050”**

**Backside Potential: Drain**

**Mask Ref: GEN 3 HEX-4 60V N-Channel**

**APPROVED BY: DK DIE SIZE .170” X .227” DATE: 7/11/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .015” P/N: IRFC044B**

**DG 10.1.2**

#### Rev B, 7/19/02